Manchester
TMS Development Platform
Technical Brief

Revision 1

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Manchester TMS Development Platform Technical Brief

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General

The Manchester development platform is a modular system based on NComm's existing TIM and STIM interfaces, which communicate through a PCIE x1 over cable interface. Manchester allows for prototyping and development by connecting a host PC running software on Windows, Linux, or other PC operating system to interface to various telecom products.

Manchester includes 4 TIM (Telecom Interface Module) connector sets with a PowerPC bus based interface. TIM TDM and UTOPIA interfaces connect to an FPGA for optional interconnect. For more advanced applications a STIM (Side Telecom Interface Module) interface is provided that includes the entire 32 bit PowerPC bus interface, along with TDM. The STIM is in the form of one DIN96 connector.

Power Interfaces

Power Input

The Manchester board has a choice of being powered by many power connection types. Only one of the connectors must be used at any one time otherwise contention may occur possibly damaging the board or power supplies. Only the +12V power and ground rails are used. All other voltages are generated on board to provide clean power regardless of the power supply used. If a connector other than the ATX input is used, then the ATX power supply must be enabled by asserting the ATX PSONL signal low external to the Manchester board. Below is a list of the power supply connector options. Refer to "Figure 1: Manchester Diagram" in Appendix for component reference designator locations.

Table 1: J5 ATX 20/24 pin Power Input Connector

Pin	Description	Pin	Description
1	+3.3V	13	+3.3V (sense)
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PSONL
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PWR_OK	20	-5V
9	+5V_SB	21	+5V

10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	GND

Table 2: P10 EPS +12V Power Input Connector

Pin	Description	Pin	Description
1	GND	5	+12V
2	GND	6	+12V
3	GND	7	+12V
4	GND	8	+12V

Table 3: P11 PCIE +12V Power Input Connector

Pin	Description	Pin	Description
1	+12V	5	GND
2	+12V	6	GND
3	+12V	7	GND
4	Unused	8	Unused

Table 4: P12 Peripheral Power Input Connector

Pin	Description
1	+12V
2	GND
3	GND
4	+5V

Power Switches

There are two power switches on the Manchester design. The main power switch SW5 when turned on enables the +12V power from any of the power input connectors to generate the on board voltages. The main reset LED at the front of the Manchester board will turn red as power is switched on. After the PCIE identifies the Manchester board, the main reset LED will turn green. Refer to “Figure 1: Manchester Diagram” in Appendix for component reference designator locations.

The second power switch SW4 is the TIM and STIM connector power switch. When the (S)TIM power switch is turned off, the TIM reset switch will turn red and the TIMS or STIM boards can safely be removed or inserted. When the (S)TIM power switch is turned on, the TIM reset switch will turn green. After the TIM switch is powered on, software must read all the TIM and STIM ID’s

to determine what boards are currently populated after the TIM power up. Refer to “Figure 1: Manchester Diagram” in Appendix for component reference designator locations.

External Power

J4 is an ATX form factor power out connector to power attached STIMS. There is an external female to female adapter to connect to the STIM power input connector with +12V, and conditioned +5V and +3.3V. Note: Although circuitry has been designed in to protect the Manchester board from having an external ATX power supply reverse power the Manchester through the STIM power output connector, avoid input power on this connector. Refer to “Figure 1: Manchester Diagram” in Appendix for component reference designator locations.

PCIE Interface

The Manchester development platform is based on the PCIE x1 over cable interface. The translation of the PCIE to the PowerPC bus is made through a PLX device namely the PEX8311. The Manchester design uses an Altera Cyclone 3 device to control the interconnect between the PEX 8311 and the TIM and STIM interfaces. There are PCIE repeaters to enable a relatively long PCIE x1 cable to be run without significant errors.

PCIE Interconnect

The Manchester board connects to the host PC PCIE adapter via an external PCIE x1 cable connecting to P9. The PCIE lanes are then buffered through a PCIE repeater. SW2 controls the PCIE repeater to compensate for different lengths of external PCIE x1 cable. The following are the DIP switch settings. Refer to "Figure 1: Manchester Diagram" in Appendix for component reference designator locations.

Table 5: SW2 PCIE Repeater Settings

SW2	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
Signal	TX SEL0	TX SEL1	TX SEL2	TX SEL3	RX SEL0	RX SEL1	RX SEL2	RX SEL3
Default	1	1	1	1	1	1	1	1

Table 6: Equalizer section

SEL0 [TX:RX]	SEL1 [TX:RX]	Compliance Channel
0	0	No equalization
0	1	[0:2.5dB] @ 1.25 GHz
1	0	[2.5:4.5dB] @ 1.25 GHz
1	1	[4.5:6.5dB] @ 1.25 GHz

Table 7: Output Swing Control

SEL2 [TX:RX]	Swing
0	1x
1	1.2x

Table 8: Output De-emphasis Adjustment

SEL3 [TX:RX]	De-emphasis
0	0dB
1	-3.5dB

Note: Testing has been done using a 5 meter external PCIE x1 cable.

PLX 8111 PCIE to PCI bridge Configuration

The PLX 8111 PCIE to PCI Bridge passes PCIE packets to the PLX 9056 PCI to Local bus Bridge.

PLX 8111 GPIO FPGA JTAG Mapping

The PEX 8111 side of the PCIE to PCI bridge has 4 GPIOs which are used to bit bang program the FPGA through JTAG. These ports must be programmed to inputs by setting the main control register 0x1020 to 0x0000000F to enable programming though the on board JTAG cable.

Table 9: FPGA Pin Configuration

GPIO Name	FPGA Connection
GPIO0	TCK
GPIO1	TMS
GPIO2	TDI
GPIO3	TDO

PLX 9056 PCI to Local bus Bridge

The PLX 9056 PCI to local bus bridge translates the PCI packets to a PowerPC type of local bus that the Manchester board uses to communicate to the peripherals on and off the board.

PLX 9056 Local Configuration Registers

The following registers can be loaded from the Local Configuration Serial Prom or programmed through the PCI interface.

0x00 Space 0 Range: Set to 0xFF000000 for 16 MB.

0x04 Space 0 Remap: set to 0x00000001 to enable to 0x0 offset.

0x18 Space 0/Exp ROM Description: Set to 0x42430040 to enable TA with 8 bit access. TAL is enabled with this register as well. **Note**: There is no ROM to configure.

0xF0 Space 1: Range: Set to 0xFF000000 for 16MB address space. This can be adjusted up to 2GB to expand STIM interface support.

0xF4 Space 1 Remap: Set to 0x80000001. to enable remap to 0x80000000 on the local bus interface. This allows expansion up to 2GB if needed.

0xF8 Space 1 Descriptor: Set to 0x00000041 to enable TA with 16 bit access for the STIM interface. **Note:** This register will need to be dynamically set depending on STIM device ID correlation. If a STIM is determined to be 32 bit wide then the value must be set to 0x00000043. If the STIM is determined to be 8 bit wide, then the value must be set to 0x00000040. TAL is enabled with this register as well.

PCI Chip Select Mapping

The FPGA decodes the local bus 32 bit address to generate the following chip selects on the board. The Manchester board uses these chip selects as defined in the table below.

Table 10:PCI Side Chip Select Associations

I/O space	Start Address	End Address	CS#	Function/Device
BAR 2	0x00000000	0x001FFFFF	CSL0	TIM Slot 0
BAR 2	0x00200000	0x003FFFFF	CSL1	TIM Slot 1
BAR 2	0x00400000	0x005FFFFF	CSL2	TIM Slot 2
BAR 2	0x00600000	0x007FFFFF	CSL3	TIM Slot 3
BAR 2	0x00800000	0x009FFFFF	CSL4	STIM (8 bit interface)
BAR 2	0x00A00000	0x00BFFFFF	Rsvd	Reserved
BAR 2	0x00C00000	0x00DFFFFF	Rsvd	Reserved
BAR 2	0x00E00000	0x00FFFFFF	Internal	FPGA registers
BAR 3	0x00000000	0x00FFFFFF	CSL5	STIM (second interface)

Local bus Chip Select Mapping

The FPGA decodes the local bus 32 bit address to generate the following chip selects on the board. The Manchester board uses these chip selects as defined in the table below.

Table 11: Local Bus Side Chip Select Connections

I/O space	Start Address	End Address	CS#	Function/Device
8 bit I/O Space	0x00000000	0x001FFFFF	CSL0	TIM Slot 0
8 bit I/O Space	0x00200000	0x003FFFFF	CSL1	TIM Slot 1
8 bit I/O Space	0x00400000	0x005FFFFF	CSL2	TIM Slot 2
8 bit I/O Space	0x00600000	0x007FFFFF	CSL3	TIM Slot 3
8 bit I/O Space	0x00800000	0x009FFFFF	CSL4	STIM (8 bit interface)
8 bit I/O Space	0x00A00000	0x00BFFFFF	Rsvd	Reserved
8 bit I/O Space	0x00C00000	0x00DFFFFF	Rsvd	Reserved
8 bit I/O Space	0x00E00000	0x00FFFFFF	Internal	On Board Registers
STIM I/O Space	0x80000000	0xFFFFFFFF	CSL5	STIM (second interface)

FPGA register map 0x00E00000 to 0x00FFFFFF

The FPGA generates its own chip select from the local bus interface which then accesses registers from within the FPGA and from I/O to the Manchester board. The register definitions are defined the table below.

Table 12: Chip Select Mapping

Address Offset	Function/Device
0x00E00000	FPGA revision
0x00E00001	Scratch register
0x00E00002	LED register
0x00E00003	DIP switch Register
0x00E00004	Interrupt Mask Register
0x00E00005	Interrupt Status Register
0x00E00006	TIM ID Low
0x00E00007	TIM ID High
0x00E00008	TIM slot LEDs
0x00E00009	Reserved
0x00E0000A	TIM slot 0 TAL timeout 2^n clk cycles
0x00E0000B	TIM slot 1 TAL timeout 2^n clk cycles
0x00E0000C	TIM slot 2 TAL timeout 2^n clk cycles
0x00E0000D	TIM slot 3 TAL timeout 2^n clk cycles

0x00E0000E	STIM slot Base TAL timeout 2^n clk cycles
0x00E0000F	STIM slot Main TAL timeout 2^n clk cycles
0x00E00010	Address bus capture byte0
0x00E00011	Address bus capture byte1
0x00E00012	Address bus capture byte2
0x00E00013	Address bus capture byte3
0x00E00014	Data Bus Capture Byte 0
0x00E00015	Data Bus Capture Byte 1
0x00E00016	Data Bus Capture Byte 2
0x00E00017	Data Bus Capture Byte 3
0x00E00018 to 0x00FFFFFF	Reserved

FPGA revision 0x00E00000

This register states the current FPGA revision

FPGA Scratch Register 0x00E00001

This register is mostly for testing and debug to determine proper communications with the FPGA.

Diagnostic LED Register 0x00E00002

This register is to write and read the diagnostic LEDs on the front right corner of the Manchester board. This is for testing and debug purposes.

Diagnostic Switch Register 0x00E00003

This register is to read the status of the diagnostic switch SW3.

Interrupt Mask Register 0x00E00004

Each interrupt has it's own interrupt mask. To enable an interrupt, set the correlating bit to zero.

Table 13: Interrupt Mask

FPGA Offset	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+0x0004	N/A	N/A	(S)TIM PWR	STIM	TIM 3	TIM 2	TIM 1	TIM 0
default	1	1	1	1	1	1	1	1

Interrupt Status Register 0x00E00005

Each TIM or STIM interface reports one active low interrupt. The STIM PWR interrupt is set after the TIM switch SW4 is turned on and the TIM reset turns green. Software will clear this bit by writing to this register.

Table 14: Interrupt Status

FPGA Offset	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+0x0005	N/A	N/A	(S)TIM PWR	STIM	TIM 3	TIM 2	TIM 1	TIM 0

TIM ID Registers 0x00E00006 and 0x00E00007

The ID registers are used to determine the types of TIM's present in the system. Typical software implementation will read the TIM ID values and assign device drivers based on the values.

Slot TIM IDs that are the value 0xe indicate an extended TIM ID. The extended TIM ID may be read at offset 0 of the slot address. A value of 0xf indicates that a TIM card is not present in the slot.

Table 15: TIM ID Rgister

FPGA Offset	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+0x0006	Slot 1 Tim ID				Slot 0 Tim ID			
+0x0007	Slot 3 Tim ID				Slot 2 Tim ID			

TIM Slot LED Register 0x00E00008

Table 16: TIM Slot LEDs

FPGA Offset	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+0x0008	TIM slot 3		TIM slot 2		TIM slot 1		TIM slot 0	

The Slot LEDs can be controlled as follows:

B”00” or B”11” – LED Off

B”01” – LED is ON and is RED

B”10” – LED is ON and is GREEN

Tim Control Register 0x00E00009

Bit 7 is the active high TIM reset. This bit initializes to a 1 for reset. This bit has to be cleared to clear the reset on the TIM and STIM interfaces

Table 17: Interrupt Status

FPGA Offset	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+0x0009	N/A	N/A	N/A	N/A	N/A	N/A	N/A	TIM RST

Transfer Acknowledge Termination 0x00E0000A - 0x00E0000F.

Each local bus transaction from the PLX device requires TAL to terminate the cycle. The registers in offsets 0x00E0000A though 0x00E0000F are the TAL timeouts which correlates to 2^(8 bit value)*20ns for each of the correlating (S)TIM interfaces. The TIM interfaces to not contain a real TAL interface, however the STIM interface can terminate the local bus cycle if the STIM TAL line is asserted low. These separate registers allow flexability in speeding up or slowing down accesses based on each TIM or STIM ID if needed. The default is set to 0x4 for 16 clock cycles at 20ns or 320ns total.

Caution: Higher values will make the PC appear to lock up since the local bus access timeout will be extremely long. Try to keep these values relatively small unless larger timeouts are required.

Local bus Address Capture 0x00E00010 - 0x00E00013.

These four registers capture the 32 bit address from any local bus cycle that does not go to the FPGA. If a local bus cycle should fail and hang the PC, then after the PC is rebooted, these register can be read to determine what caused the failure.

Local bus Data Capture 0x00E00014 - 0x00E00017.

These four registers capture the 32 bit data from any local bus cycle that does not go to the FPGA. If a local bus cycle should fail and hang the PC, then after the PC is rebooted, these register can be read to determine what caused the failure.

Telecom Interface Module (TIM Interface)

The Manchester development platform contains four TIM interfaces. Each of the TIM interfaces consists of three 50-position connectors; the table below shows the pin names for the connectors. Refer to “Figure 1: Manchester Diagram” in Appendix for component reference designator locations.

Table 18: TIM Connector Pin Definitions

P1X00 (X=slot +1) MAIN LOCAL BUS		P1X01 (X=slot +1) TDM AND BUSSES		P1X02 (X=slot +1) UTOPIA	
Pin	Signal	Pin	Signal	Pin	Signal
1	+5 V	1	+5 V	1	TXADDR[3]/TXCLAV[2]
2	GND	2	GND	2	TXADDR[4]/TXCLAV[3]
3	NIMX_0	3	SNIM_NX_0	3	TXADDR[1]
4	A31	4	SNIM_B0	4	TXADDR[2]/TXCLAV[1]
5	NIMX_1	5	SNIM_NX_1	5	GND
6	A30	6	SNIM_B1	6	TXADDR[0]
7	NIMX_2	7	SNIM_NX_2	7	TXDATA[6]
8	A29	8	SNIM_B2	8	TXDATA[7]
9	NIMX_3	9	SNIM_NX_3	9	TXDATA[4]
10	A28	10	SNIM_B3	10	TXDATA[5]
11	NIMX_4	11	SNIM_NX_4	11	TXDATA[2]
12	A27	12	SNIM_B4	12	TXDATA[3]
13	NIMX_5	13	SNIM_NX_5	13	TXDATA[0]
14	A26	14	SNIM_B5	14	TXDATA[1]
15	NIMX_6	15	A21	15	TXPRTY
16	A25	16	SNIM_B6	16	TXENA
17	NIMX_7	17	A20	17	TXSOC
18	A24	18	SNIM_B7	18	TXCLK
19	NIMX_8	19	A19	19	GND
20	A23	20	D15	20	GND
21	NIMX_9	21	A18	21	TXADDR[3]/TXCLAV[2]
22	A22	22	D14	22	TXADDR[4]/TXCLAV[3]
23	NIMX_10	23	+3.3 V	23	TXCLAV[0]
24	RHWL	24	D13	24	TXADDR[2]/TXCLAV[1]
25	NIMX_11	25	CLK16384MHZ	25	GND

TIM Connector Pin Definitions continued

26	GND	26	GND	26	GND
27	NIMX_12	27	+3.3 V	27	RXADDR[3]/RXCLAV[2]
28	BWE0L	28	D12	28	RXADDR[4]/RXCLAV[3]
29	NIMX_13	29	A17	29	RXADDR[1]
30	HRESETL	30	D11	30	RXADDR[2]/RXCLAV[1]
31	NIMX_CSL	31	A16	31	GND
32	CPUCLK5	32	D10	32	RXADDR[0]
33	NIMX_ID0	33	A15	33	RXDATA[6]
34	D7	34	D9	34	RXDATA[7]
35	NIMX_ID1	35	14	35	RXDATA[4]
36	D6	36	D8	36	RXDATA[5]
37	NIMX_ID2	37	A13	37	RXDATA[2]
38	D5	38	FPGAOEL	38	RXDATA[3]
39	NIMX_ID3	39	A12	39	RXDATA[0]
40	D4	40	BWE1L	40	RXDATA[1]
41	CLK44736MHZ	41	A11	41	RXPRTY
42	D3	42	GND	42	RXENA
43	NC	43	+2.5 V	43	RXSOC
44	D2	44	CLK1544MHZ	44	RXCLK
45	IRQL (n/a)	45	+5 V	45	GND
46	D1	46	GND	46	GND
47	IRQL	47	CLK20MHZ	47	RXADDR[3]/RXCLAV[2]
48	D0	48	CLK3088MHZ	48	RXADDR[4]/RXCLAV[3]
49	+5 V	49	+5 V	49	RXCLAV[0]
50	GND	50	GND	50	RXADDR[2]/RXCLAV[1]

Side Telecom Interface Module (STIM Interface)

To provide expanded capabilities to the Manchester design a STIM interface is provided. The STIM interface provides the entire 32 bit local bus bus from the PCI bridge, along with a TDM channel and various system generated clocks. The interface is comprised of one 96-position DIN connector. The complete pin description can be found in the table below. Refer to "Figure 1: Manchester Diagram" in Appendix for component reference designator locations.

Table 19: STIM Pin Description

Pin	J1 Connector		
	Row A	Row B	Row C
1	D31	+5 V	D15
2	D30	+5 V	D14
3	D29	A31	D13
4	D28	A30	D12
5	D27	A29	D11
6	D26	A28	D10
7	D25	A27	D9
8	D24	GND	D8
9	D23	A26	D7
10	D22	A25	D6
11	D21	A24	D5
12	D20	A23	D4
13	D19	A22	D3
14	D18	GND	D2
15	D17	A21	D1
16	D16	A20	D0
17	CLK16384MHZ	A19	RCLK
18	ALE	A18	TCLK
19	TSYNC	A17	RXD
20	RSYNC	GND	TXD
21	RAMPSDA10	A16	RAMCAS
22	RAMWEL	A15	RAMGL4L
23	CS5L (Main)	A14	RAMPSDAMUX
24	CS4L (Base)	A13	CLK1544MHZ
25	RHWL	A12	TAL
26	OEL	GND	TEAL

27	+5 V	A11	HRESET
28	+5 V	A10	IRQ7L (n/a)
29	WE0L	A9	IRQ4L
30	WE1L	A8	IRQ1L (n/a)
31	WE2L	A7	IRQ0L (n/a)
32	WE3L	GND	CPUCLK4

Program and Debug Interfaces

There is an Altera byte blaster interface connector to be able to program the Altera FPGA. There is also an active serial connector to be able to program the configuration SPROM for the FPGA. There is a set of dip switches (SW3) and a set of LEDs (CR3-CR10) connected to the local bus that software can use for debug as needed. Refer to "Figure 1: Manchester Diagram" in Appendix for component reference designator locations.

Table 20: FPGA JTAG Connector P7

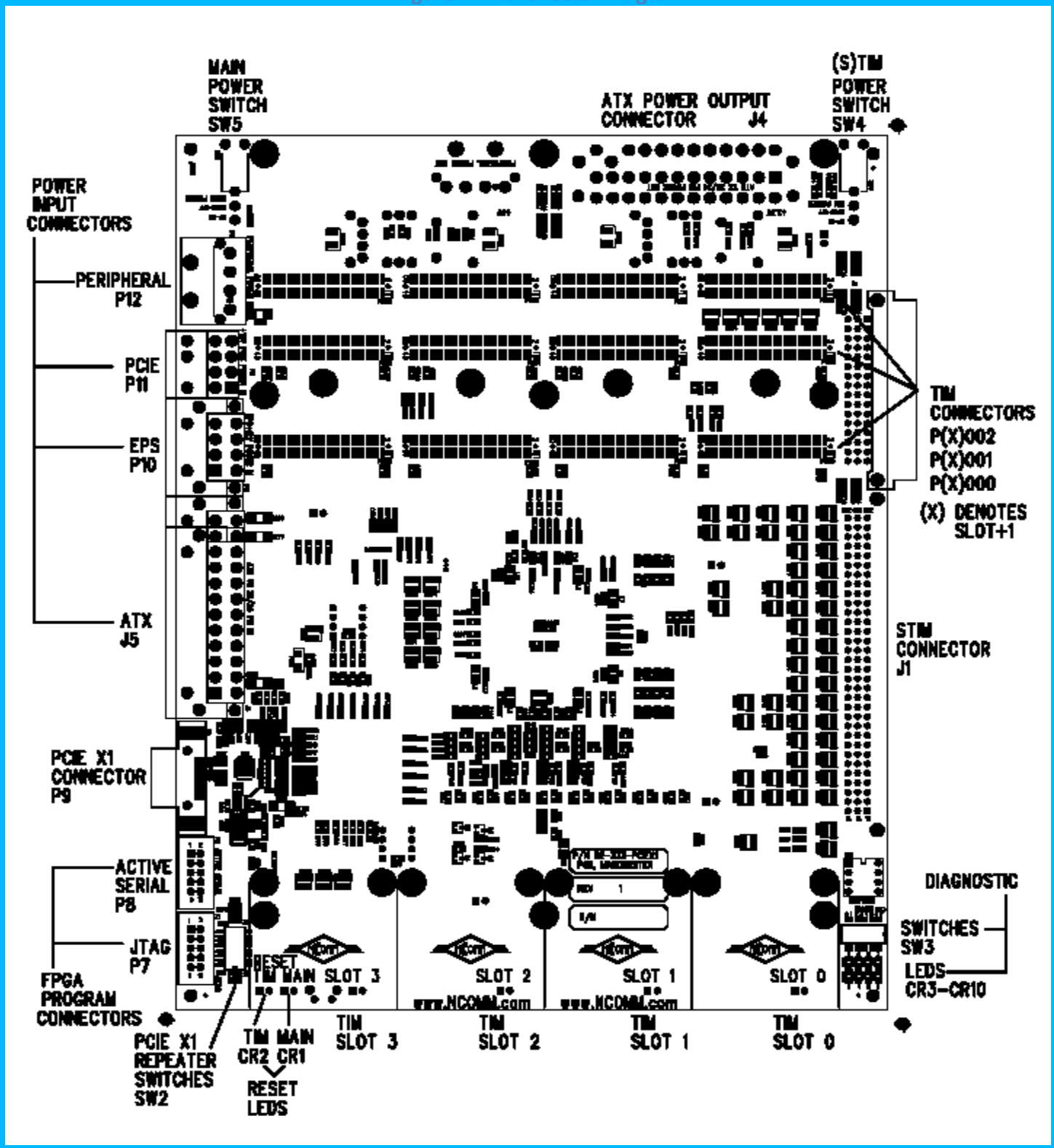
Pin	Description	Pin	Description
1	TCK	2	GND
3	TDO	4	+3.3V
5	TMS	6	N/C
7	N/C	8	N/C
9	TDI	10	GND

Table 21: FPGA AS (Active Serial) Connector P8

Pin	Description	Pin	Description
1	DCLK	2	GND
3	INIT_DONE	4	+3.3V
5	NCONFIG	6	NCE
7	DATA	8	CSL
9	ASDI	10	GND

Appendix

Figure 1: Manchester Diagram



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